NASA CR-145204

FINAL REPORT

Further Development of an Indium Antimonide (InSb) Charge-Coupled Infrared Imaging Device (CCIRID), 20-Element Linear Imager

Contract No. NAS1-14395

For - National Aeronautics and Space Administration
Langley Research Center
Hampton, Virginia 23365

SANTA BARBARA RESEARCH CENTER
A Subsidiary of Hughes Aircraft Company
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15 April 1977

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Section 1
INTRODUCTION

The development of Indium Antimonide (InSb) Charge-Coupled Infrared Imaging Devices (CCIRIDs) by Santa Barbara Research Center has proceeded under NASA contract for four years. The use of charge-coupled devices (CCDs) for infrared (IR) imaging allows signal processing to be achieved in real time directly on the focal plane. This type of processing results in significant reductions in the IR sensor weight and power requirements, both prime advantages for applications such as remote earth sensing and outer planet exploration.

The feasibility of the concept[1] was demonstrated under NASA contract NAS1-12087. During this contract, InSb MIS devices were fabricated and tested to establish the requisite processing parameters for an InSb CCD. The success of this effort led to the design of a 9-bit CCD mask set (8580) complete with other test structures for process control. Dimensional and multilayer requirements for CCDs were demonstrated for the InSb system with this mask set.

Development of the InSb processing technology[2] continued under NASA contract NAS1-13163. In this effort, the important milestone of charge transfer with proper time delay was achieved in an 8580 InSb CCD. A charge transfer efficiency (CTE) of 0.90, which was low due to the extreme gate lengths of the 8580 design, was measured and provided the impetus for a new mask set (8582) design with reduced gate lengths.

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1. "Charge-Coupled Infrared Imaging Device (CCIRID) Feasibility Study," Final Report NASA CR-132383, Contract No. NAS1-12087, December 1973.
2. "Development of InSb CCD for Infrared Imager Applications," Final Report NASA CR-132694, Contract No. NAS1-13163, May 1975.

The successful operation[3] of the 2-bit structure of the 8582 design marked the continuing process development during contract NAS1-13937. The gate lengths of this structure as well as the 9-bit CCIRID imager of the 8582 are 25.4-μm (1.0 mil), reduced from the 50.0-μm (2.0 mil) values of the 8580 chip. As a result of this change, improvement in CTE values to CTE = 0.99 were predicted for storage well depths of 2.0 volts. The observed value of $\alpha \simeq 0.975$ agreed well with this prediction, particularly since the predicted value for a 1.0-volt well depth (approximately the observed value) was 0.983.

Despite this important achievement, the lack of a similar demonstration for the 9-bit imager was a setback. The reasons behind this failure were identified as arising from 1) design flaws in the 8582 mask set, and 2) difficult topological steps formed in the CCIRID structure due to the CCD process sequence. Steps have been taken in the present contract (NAS1-14395) to resolve these problems. In Section 2, the steps taken to remove these barriers to successful operation of the 9-bit imager are discussed. In particular, the redesign of the 8582 mask set and InSb process development are discussed.

The design of the next generation CCIRID structure, the 8585, is addressed in Section 3. This new mask set utilizes 12.5-μm gate lengths in the CCD shift registers, thus providing for more efficient transfer of charge (CTE ≃ 0.999) through the registers. Incorporating 1) a 20-element 4φ linear imager, 2) 4-element 4φ time-delay-and integration (TDI) array, 3) a 4-element 2φ linear imager, and 4) a monolithic gated charge integrator output circuit, this new chip design provides test vehicles for all major CCD imaging structures which are likely to be important for future NASA applications.

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3. "Development of InSb Charge-Coupled Infrared Imaging Device -- Linear Imager," Contract NAS1-13937 (NASA CR-145003), April 1976.

To process the new design in an optimum fashion, a total etch CCIRID process sequence is required. Although some problems remain in achieving high yield, important progress has been achieved in the past year primarily through internally (SBRC) funded programs and particularly a second externally funded[4] program. The nature of these improvements is summarized in Section 2. All CCDs fabricated in the future will use planar InSb diodes on the CCD and a total etch procedure.

Finally, the impact of a InSb CCIRID for NASA applications is described in Section 4. The application chosen for this illustration is that of a future LANDSAT system, but the same analysis is applicable to other similar systems.

In Section 5, the conclusions drawn from the investigations of this contract are presented.

4. HALO Monolithic Intrinsic Detector/MUX Array Program, Contract No. F04701-76-C-0174.

Section 2

CCIRID FABRICATION AND TESTING: 8582

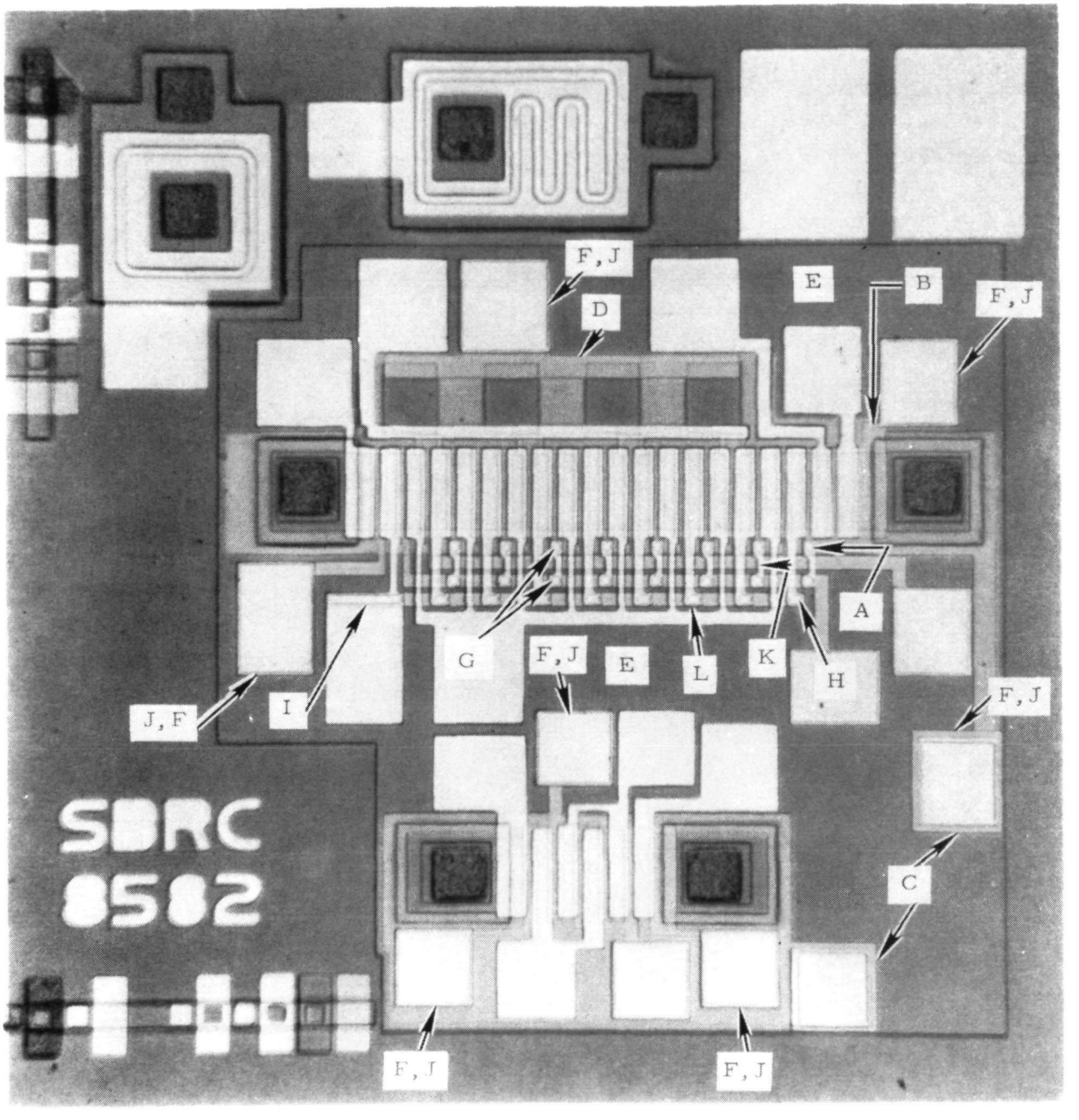
The 8582 CCIRID, designed under NASA contract NAS1-13163, has been the object of intensive study during this contract period. The original design was demonstrated, during contract NAS1-13937, to possess several flaws which were decreasing the chances for an operational 8582 imager. As a result, a redesign of the pertinent mask layers was undertaken. The extent and success of this effort will be considered in the following along with considerations of InSb CCIRID processing technology.

REDESIGN OF 8582

As a result of the studies during the previous contract period, it was established that a major failure mode for the 8582 9-bit imager was the breaking of the surface metal clock lines (ϕ_1, ϕ_2, and surface metal jumper line for the ϕ_2 clock) at the steps formed by the buried metal insulator.

A redesign effort concerned exclusively with eliminating these problem areas in the existing 8582 mask set was thus carried out in this contract period. The mask levels affected were the buried metal (layer 4), buried metal insulator (layer 5), and the surface metal (layer 10). With the problem areas of concern being "microcracks" in metal lines at oxide steps and/or breakage of such lines at the edges of mesa diodes, the changes in the layers were such as to minimize the occurrence of this type of phenomenon in future fabrication runs.

On the buried metal layer, the revisions are indicated in Figure 1, a photograph of a completely processed 8582 chip incorporating the mask changes under discussion. Revision [A] effectively broadens the ϕ_2 buried metal strips and was made to all strips in the channel -- not just the strip indicated. The intent of this revision is to ensure a good contact between these strips (defining the ϕ_2 clock line) with the ϕ_2 bus bar. This contact



A - D Changes in Buried Metal Layer
E - I Changes in Buried Metal Insulator Layer
J - L Changes in Surface Metal Layer

Figure 1. 8582 Chip Illustrating Design Changes in Photomask Layers

is made by a surface metal strip to be discussed later. To minimize the breakage of the output buried gate line at the mesa diode edge, revision [B] was made. Note that the pattern for this line now completely covers the diode edge. Revision [C] results in a layer of buried metal being added to the channel stop metal pads. This change enables the 8582 mask set to be used for normal etch technology as well as the baseline technology of reverse photolithography. Finally, the photogate bus bar (Revision [D]) was extended as indicated. This change should ensure continuity of the bus bar along the detector array.

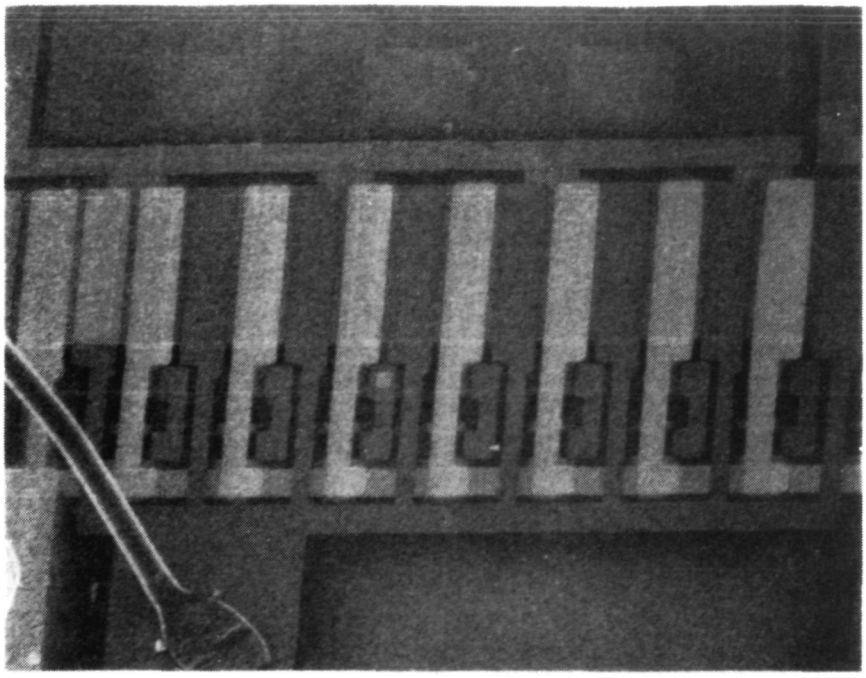
Revisions to the buried metal insulator mask are compatible with these changes to level 4, and are also shown in Figure 1. The most obvious change is the extension of the insulator [E] to cover the entire active area of the chip. This extension ensures the elimination of oxide steps and should, therefore, greatly increase the yield of 8582 processing. To achieve this extension, it was necessary that previously defined buried metal pads (now including the channel stop pads by virtue of [C]) be left open [F] for future probe contact. This opening was made smaller than the pad so that an etch technology compatibility was achieved. To replace the oxide steps formed by the previous design of this layer, contact windows [G] and [H] are now left in the insulator. Again the window sizes are smaller than the underlying buried metal patterns (the width increase in the buried metal strips [A] ensures this point) for etch compatibility. For completeness, it may be noted that the windows [G] are for the ϕ_2 line surface metal jumper while windows [H] are required for the contacts of the ϕ_1 clock lines. By virtue of the extension of the insulator over the active area, it is clear that the steps originally encountered by the ϕ_3 line have been totally eliminated. The use of contact windows likewise minimizes the impact of "microcrack" phenomenon in delineating the surface metal pattern. Finally, note that the window [I] is required for making contact to the buried metal bus bar of the ϕ_1 clock line.

The final revisions are those to the surface metal pattern — level 10 — and are also indicated in Figure 1. Again surface metal is left over all pads [J] now for etch process compatibility. The remaining changes are evident in the case of [K] and [L]. Revision [K] was necessary to accommodate the previously noted changes to the buried metal and buried metal insulator levels. This ensured that the step coverage problems previously observed for this line are no longer a factor in limiting device yield. Similarly, the revision [L] in the ϕ_1 clock line pattern eliminated step coverage problems. It should be noted here that the above revisions constitute the maximum changes which can be made on the 8582 mask set without undertaking a complete revamping of all layers.

FABRICATION AND TEST OF 8582

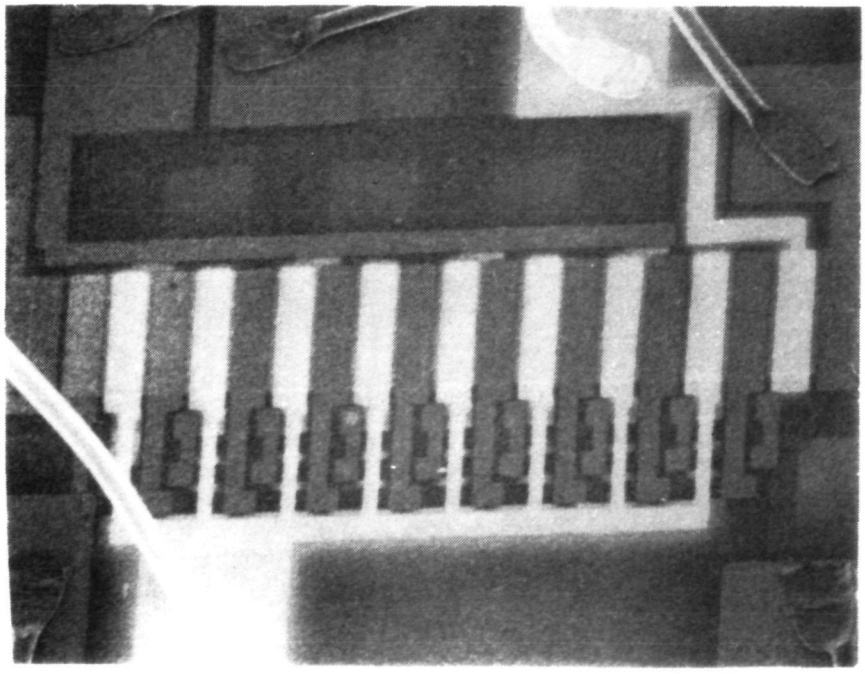
After receiving the revised photomask plates, several 8582 fabrication lots were processed using the reverse lithographic technique. Representative chips from each lot were then examined with a scanning electron microscope operating in the voltage contrast mode. In this mode, the InSb substrate is shorted to the CCD diodes and a bias voltage (ΔV_c) is then applied between these elements and the selected CCD component such as the ϕ_1 or ϕ_2 clock line. The value of ΔV_c, in the present discussion, is not germane and will thus not be quoted quantitatively. It is specified in the various cited figures. These investigations revealed 1) that the redesign was successful in eliminating the microcracks of the surface metal clock lines, but 2) that there remained process related problems which continued to limit the yield of operative devices.

The success of the redesign is illustrated in Figures 2, 3, and 4. In Figure 2, the electrical continuity of the ϕ_1 lines illustrates not only the elimination of microcracks, but the success of the interlayer contact windows between the surface metal lines and the buried metal strip from the ϕ_1 pad.



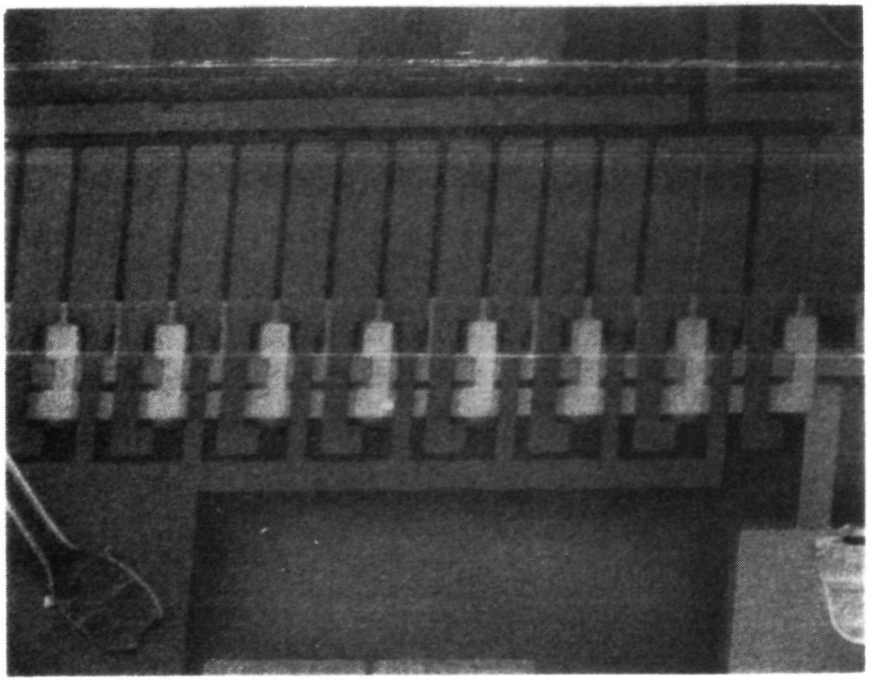
ϕ_1: -6V All other gates grounded to substrate

Figure 2. Voltage Contrast Photograph (145×) of ϕ_1 Clock Line Electrical Continuity: Revised 8582 Design



ϕ_3, ϕ_{3i}: -9V All other lines grounded to substrate

Figure 3. Voltage Contrast Photograph (110×) of ϕ_3, ϕ_{3i} Clock Line Electrical Continuity: Revised 8582 Design



$\phi_{2,4}$: -9V All other lines grounded to substrate

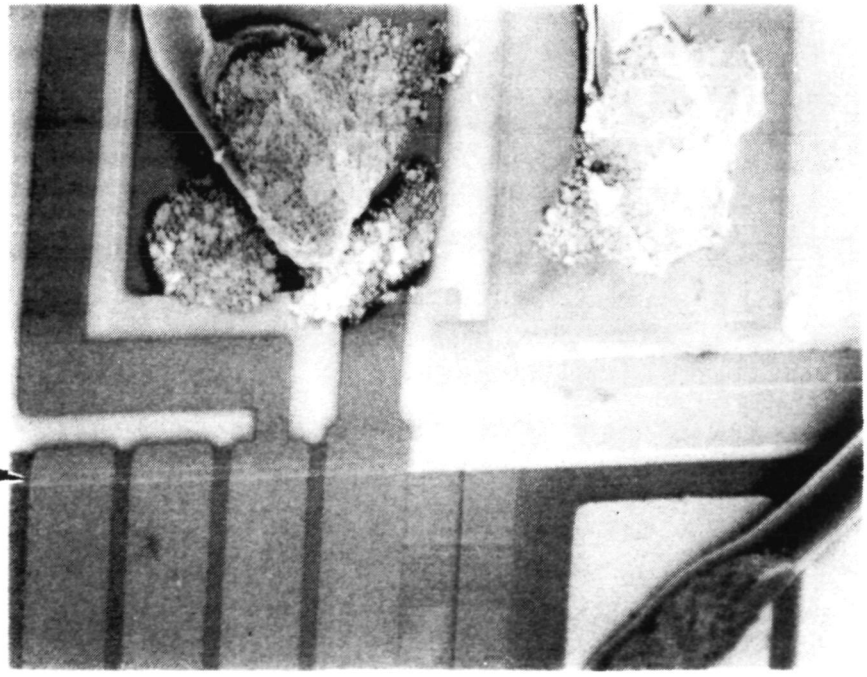
Figure 4. Voltage Contrast Photograph (145×) of ϕ_2 Clock Line with Revised 8582 Design. Note Continuity of Surface Metal Jumper Bars.

The similar success for the ϕ_3 and ϕ_{3i} surface metal clock lines is shown in Figure 3. Since both ϕ_1 and ϕ_3 exhibited a severe breakage (approximately 10% of all lines on a given device were open due to microcracks) phenomenon, and hence lack of electrical continuity prior to the redesign, it is apparent that this problem has been corrected.

A similar difficulty with the ϕ_2 surface metal jumper bars also existed and is likewise eliminated in the new design as evidenced by Figure 4. This Figure shows a portion of the CCD channel region with both ϕ_2 and ϕ_4 buried metal clock lines biased negatively with respect to the substrate. The continuity of the ϕ_2 jumper bars and the success of all the interlayer contacts are evident. The prime remaining problem area is also evident in this figure, however, and that is the failure of either the ϕ_2 (only two gates do not break) or the ϕ_4 (no continuous gates) to traverse the step formed at the channel edge by the channel stop insulator layer. This step is similar to

that originally (before the redesign) present at the edges of the buried metal insulator so that a problem here is not entirely unexpected. The unfortunate surprise is the greater extent of the breakage at the edge for the buried metal (rather than surface metal) lines.

The extent of the problem is further illustrated in Figure 5 where the new design of the ϕ_{OB} gate as well as its failure to traverse the channel stop insulator step is shown. The channel edge is marked in the Figure, and it should be observed that the continuity break is at this edge, not at the mesa diode. The nature of the problem at this edge is shown in detail in Figure 6. This figure shows an SEM photograph (7800× magnification) of the channel edge with the channel stop metal, channel stop insulator, and $\{\phi_1, \phi_2, \phi_3\}$ clock lines indicated. The break in the ϕ_2 line at the channel stop insulator edge is evident.



ϕ_{OB}: -9V All other lines grounded to substrate.
Note charging of oxide.

Figure 5. Voltage Contrast Photograph (220×) of ϕ_{OB} Control Gate: Revised 8582 Design

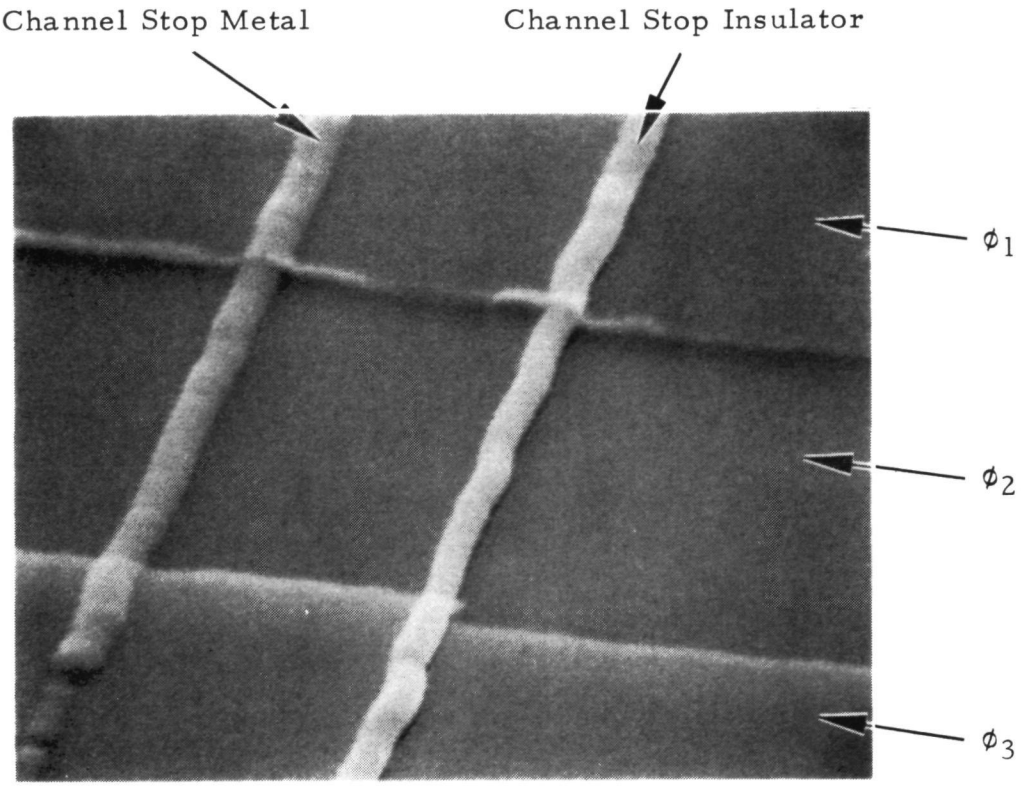


Figure 6. Voltage Contrast Photograph (7800×) of CCD Channel Edge. Note Break in ϕ_2 Line at Channel Stop Insulator Edge.

It is then apparent that the processing sequence for the 8582 structure must be altered to achieve a significant yield of operative chips. This statement assumes that complete revamping of all 8582 layers is not a desirable option. One possible alternative to the present reverse photolithographic mode of processing is to convert all masks in the 8582 set to be compatible with a total etch processing sequence. As previously noted, the revisions to the 8582 layers (4, 5, 10) were made in such a way that a total etch compatibility is assured. The remaining levels that were not changed (with the exception of the previously redesigned channel stop metal layer) are not compatible with the etch approach. The lack of compatibility is most troublesome due to the presence of mesa – rather than planar – diode structures in the component technology that was available during the performance period of this contract.

Significant progress has been made toward the achievement of such a process, and this progress will be summarized later in this report. For now, it is sufficient to note that for the period of performance on this contract, an etch process was not available and a second alternative was required.

For the interim period of this contract, it was necessary to consider alternatives to the total etch procedure which would also solve the problem posed by the step at the CCD channel edge. The result was the concept of a Buried Channel Stop (BCS) illustrated in Figure 7. It may be seen that the channel stop insulator (CSI) is effectively eliminated in this scheme by depositing the gate insulator in two stages. The removal of the CSI step would be expected to remove any breakage problems of the clock lines at the channel edges. Nevertheless, potential problems do exist with the BCS process. First, the field oxide which supports all circuitry external to the CCD channel is virtually identical with the gate insulator in thickness. As a result, capacitive feedthrough and/or oxide leakage may pose a greater problem than heretofore observed. This prospect is made even greater with the mesa diode requirement of gate control for larger reverse breakdown voltages and lower leakages. Thus the proper bias on the diode gate (which function is served by the channel stop metal) is opposite to the bias required for a proper channel stop region being created at the CCD channel edge. A second potential problem is the small separation of 1) the channel stop metal from the substrate and 2) the channel stop metal and the buried metal. The first separation, identified by oxide 1 in Figure 7, could result in a greater incidence of shorts to the InSb substrates since it evidently places a more stringent requirement on oxide quality than a 0.15- or 0.20-μm layer. Similarly, the decreased oxide thickness between the channel stop metal and the buried metal places severe restrictions on oxide quality. Finally, the existence of the interface between oxides 1 and 2 could lead to fixed charge enhancement over the singly oxidized structures. Such a difficulty should not, however, be a severe limitation on processing yields.

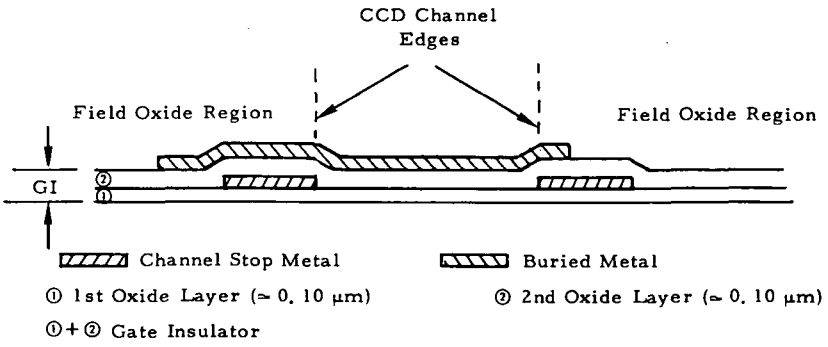
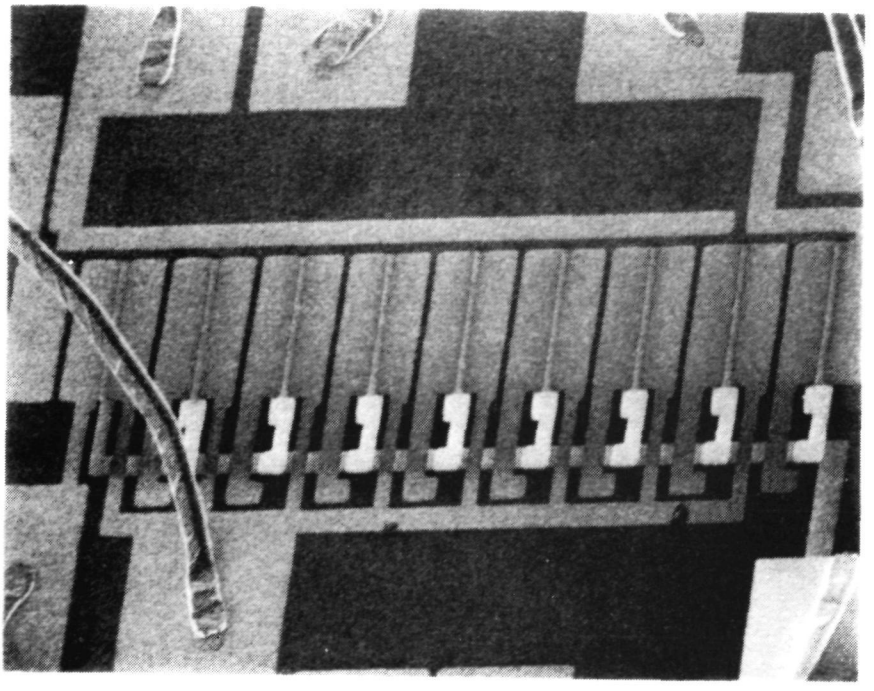


Figure 7. Buried Channel Stop Process – Schematic

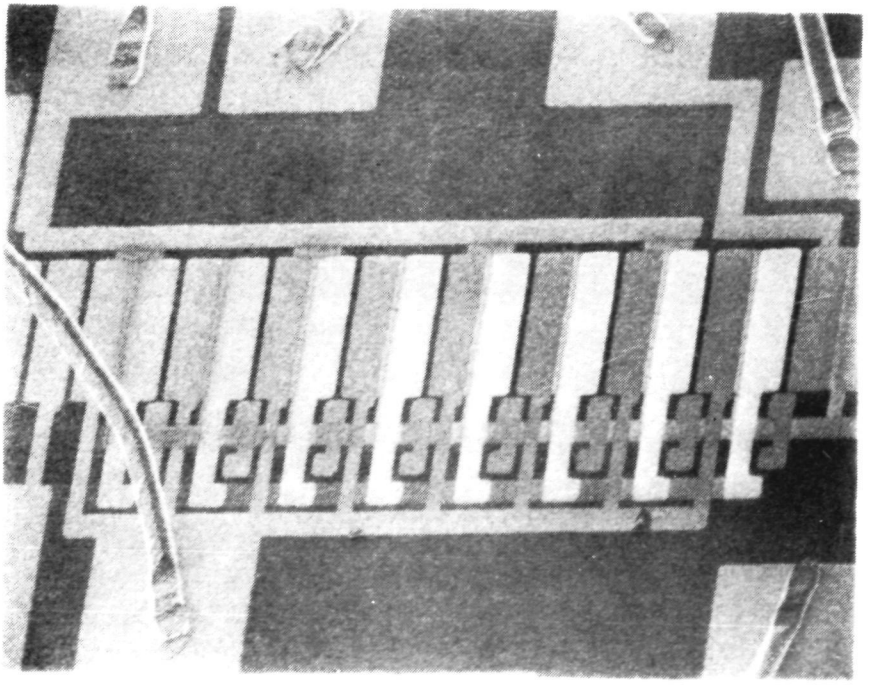
Despite these potential problems, several wafer lots were fabricated for the 8582 mask set using the BCS process. Of the resulting candidate die, only 177 of 600 possible 9-bit devices were subjected to dc test due to lack of time in this contract period. Of those subjected to such a test, approximately 62% failed due to some type of dc short to the InSb substrate. Most of these were shorts between the channel stop metal and the substrate, but not all. The remaining failures were due to the normal incidence of gate-to-gate shorts and were not unusual although the incidence of photogate (ϕ_p) to channel stop metal shorts were somewhat higher than in the past. The overall yield of good (pass dc test) was thus 7.3%.

Voltage contrast studies of these BCS processed devices reveal that the coverage problem is removed. In Figures 8 and 9, this point is made quite clear by the clear electrical continuity of the ϕ_2 and ϕ_4 clock lines. Note in Figure 9 that the ϕ_4 clock line is also shorted to the ϕ_1 clock line. Since it was not worthwhile to subject those die which had passed the dc screen test to the SEM probe, devices which had failed that test with only one short were used for the voltage contrast studies. It is evident that the one short of the die in Figure 9 was of a ϕ_1 - ϕ_4 gate-to-gate variety, an observation consistent with the dc screen test procedure. In lieu of additional figures, it is sufficient to note here that all the other buried gates showed similar continuity at the channel edge. As a result, it is clear that the BCS process does remove the major remaining obstacle to operative 8582 9-bit devices.



ϕ_2: -16.5V All other lines grounded to substrate

Figure 8. Voltage Contrast Photograph (120×) of ϕ_2 Clock Line on Device Processed by BCS Technique. Note complete Electrical Continuity of all ϕ_2 Lines.



ϕ_4: -16.5V All other lines grounded to substrate

Figure 9. Voltage Contrast Photograph (120×) of ϕ_4 Clock Line Processed by BCS Technique. Note Full Continuity of the Lines Across the CCD Channel.

Due to a lack of time remaining in this contract period, it was not possible to test all the devices which qualified as candidates for ac test. Four devices were tested. Of these four, two failed almost immediately with a diode short in one case and a channel stop metal-to-substrate short in the other. The remaining devices exhibited no obvious failure mechanisms although the diode leakage current was high, being approximately 1 μa for a 1-volt reverse bias. To achieve this value, it was necessary to use gate control of the diode by means of the channel stop metal and the output buried gate (or the input surface gate in the case of the input diode). A channel stop (V_{cs}) bias of approximately -1.5 volts relative to the InSb substrate was required. Since this polarity is the reverse of that required for optimum operation of V_{cs} as a channel stop, it is evident that a compromise must be made in balancing these two functions of the channel stop metal.

If it is assumed that this bias configuration is adequate to ensure channel isolation from the remainder of the InSb chip, then the 1-μa leakage current is the correct value for the output diode. But for this current and a 10-kHz operating rate in the device, the charge leakage to the substrate is

$$Q_L \approx (10^{-4}\text{sec}) \times (1 \times 10^{-6}\text{A})$$
$$= 10^{-10}\text{coul} = 100 \text{ pc}$$

This number must be compared to the charge storage capacity of an individual CCD well. A typical value for the well depth (ΔV_w) is about 1 volt and the area of an individual gate is approximately $3.87 \times 10^{-5}\text{cm}^2$. Since the gate insulator capacitance (buried metal) is approximately $2.5 \times 10^4\text{pf/cm}^2$, the maximum charge stored is

$$Q_{max} \approx C_{ox}A_w\Delta V_w = 0.9675 \text{ pc} \approx 1.0 \text{ pc} \quad (1)$$

which is nominally a factor of a 100 lower than the projected leakage charge.

An additional requirement is that the leakage current not be sufficiently large that the preset reverse bias of the diode is completely discharged. Since a 1-volt reverse bias was the maximum possible, it is clear that the charge preset on the output diode capacitance ($\lesssim$ 10 pf) is

$$Q_{pset} \approx (1V) \times (10\ pf) = 10\ pc$$

It follows at once that the high leakage of 1μa could easily prevent retention of a nominal 1-volt reverse bias on the output diode. The result is then the total inability to detect charge from the CCD register.

Even if the leakage charge were negligible, the disparity of a CCD well storage capacitance and the 8582 output diode capacitance will minimize the observable signal. In particular, the output diode must be bonded directly to an external circuit for amplification of the CCD signal due to lack of an on-chip circuit. The resulting parasitic capacitance adds to that of the diode itself ($\simeq$4 pf) to produce a net output capacitance of between 8 and 10 pf. For the worst case, a 1-volt charge packet in the CCD register ($C_{gate} \simeq 0.97$ pf) will provide only 0.097 volt (maximum) at the device output. Thus

$$\begin{aligned} Q_{register} &= (C_{ox}A_w)\ \Delta V_w = C_{out}\ \Delta V_{out} \\ \text{or} \qquad \Delta V_{out} &\cong \frac{1.0\ pc}{10\ pf} = 0.1\ volt \end{aligned} \tag{2}$$

Since this value is further reduced by the gain ($\simeq$ 0.8) of the output detection stage, it is clear that a 1-volt signal will produce only an 80-mv output or less. This magnitude can be easily detected, but the numbers indicate the degree of signal reduction to be expected on the basis of the size of the output diode. This feature has been reduced considerably on the new CCIRID chip and an 800-mv output should be achievable. Only a total 8582 redesign can remove this troublesome problem area for the 9-bit imager.

When reviewing the test results, it should be remembered that only four devices out of the available die were extensively tested for CCD operation. Further, these devices were from the same wafer suggesting the possibility of degraded diodes on all die from that wafer. If the remaining BCS wafers

are examined, devices with significantly lower diode leakage characteristics may be obtained allowing final characterization of the 8582 CCD imager.

CCIRID PROCESS DEVELOPMENT

The desirability of a total etch CCIRID process has been previously mentioned. With the aid of internal (SBRC) funding programs and particularly the benefits of a second externally funded[4] program, a great improvement in such a process has recently been realized. The following paragraphs summarize the nature of these improvements.

Planar p-n diodes have recently been fabricated on InSb using ion-implantation of beryllium ions. Initial data indicate high reverse breakdown voltages for these junctions ($V_R \simeq 4$ to 6 volts), better than obtained with the heretofore used mesa diode structures. This increase is especially promising from the standpoint of "on-chip" charge packet detection and processing. It would appear that continued development will yield high quality planar junctions with all the attendant topographic advantages for multi-level CCIRID structures.

The requisite gate insulator technology has also shown rapid improvement with insulators possessing flat-band voltages of approximately -0.5 volt (n-type InSb substrate), interface state densities of $2 \times 10^{11}/cm^2$-ev at mid-gap, and negligible hysteresis. Current development efforts are concentrating on the requirement that each individual process step (e.g., p-n junction, gate insulator) must be compatible. This integration should be complete shortly so that future CCIRID processing will be via a total etch technology.

Finally, an internally funded program, working in association with the NASA Langley Research Center, is currently under way to develop a fully planar channel stop structure. The approach utilizes ion-implantation, and the principal effort will be to identify an ion or ions which can form an n^+ ($\simeq 10^{18}/cm^3$) layer overlying an n-type InSb substrate. Once this demonstration has been made, then the integration of the planar channel stop into the

CCIRID process can be made. It must be pointed out, however, that implementation of this new structure will require extensive changes in some of the existing photomask designs, notably the CCIRID 8585.

Section 3
CCIRID: 8585

DESIGN OF 8585

The necessity of designing a new CCIRID structure is evident, even if a fully operational 8582 imager is obtained, if one is to truly exploit the potential of IR imaging via CCDs. Indeed, the 8582 structure has already provided valuable insight into the design problems of a CCIRID; for that reason alone it has served a significant function. The next generation imager should thereby capitalize on the information gained from the 8582 experience.

This new CCIRID chip is termed the 8585 and contains the following elements:

1. 20-element linear imager
2. 4-element linear imager
3. 2-element linear imager
4. 4-element TDI array
5. Monolithic Gated Charge Integrator (GCI)
6. Test devices

Of these structures, numbers 1, 3, and 4 are all 4ϕ devices with 12.5-μm (0.5-mil) gate lengths in the cases of 1 and 4; device 3 has 10.0-μm (0.4-mil) gate lengths. Device number 2 is a 2ϕ structure with 12.5-μm gate lengths. The test devices consist of three capacitors differing only in the metal for their gate — either channel stop, buried, or surface metal. There are, in addition, two gated diodes to aid in evaluating process parameters. To include these structures on a single chip required an increase in chip size for the 8585 as compared to the 8582 chip. The 8585 chip size is 2388 μm (94 mils) by 2896 μm (114 mils).

Finally, it is to be emphasized that the new design is for a baseline total etch (normal lithography) process technology. The design includes 11 photomask levels including two channel stop insulator layers. Although

these may not be required due to the promise exhibited by the BCS process sequence, it does provide for: 1) a smaller step at the CCD channel edge and, by means of the second CSI, 2) a thick field oxide for the pad lines. There are four metal layers — channel stop, buried, surface, and the "transparent" gates of the detectors — and two additional insulator layers, i.e., the buried metal insulator and the final pad contact overglass. The remaining three layers are: 1) the key mask for the basic alignment of the succeeding levels, and 2) the diode and the diode contact photomasks.

One fabrication run based on a total etch technology has been made at this time. Problems in the process have impacted the yield, but problems were expected since this trial constituted the first lot processed with the total etch concept. Despite the low yields, some individual devices may be functional; these will be tested as soon as possible. In the interim, these devices serve as good vehicles for the discussion of the pertinent devices on the 8585 chip.

The 20-element linear imager is shown in Figure 10. The device is a 4ϕ, overlapping gate design as shown schematically in Figure 11. This schematic diagram illustrates the basic circuitry of the CCD readout register, and the means by which optical information (stored under ϕ_P) is transferred (by pulsing ϕ_T) into a ϕ_4 well of this register. It is also to be noted that an isolated gate, ϕ_F, is provided in the design to allow for a floating clock type output. If a conventional floating diffusion output is used, then the ϕ_F line can be shorted to ϕ_2 for optimum 4ϕ clock conditions.

The input and output diodes are of the planar type with 625 μm^2 (1 mil^2) as their nominal area. This reduction in size in comparison with the 8582 structure yields a capacitance load at the output of approximately 0.1 pf. Note that the ϕ_2 clock line runs between the individual detector elements rather than being on the same side as the remaining clock lines. This change eases the complexity of clock line overlap and should result in a considerable reduction in gate-to-gate short problems. The gate lengths in the device are 12.5 μm (0.5 mil) while the channel width is 101 μm (4.0 mils).

It is a 4ϕ CCD with a "fill and spill" input structure consisting of: 1) input (ID) diode, 2) signal (B) gate, 3) surface (SC) control gate, and 4) a storage gate which is also the first ϕ_2 well. This input structure, to be discussed in detail later in this report, allows the introduction of electrical input into the CCD register which varies linearly with the signal bias applied to the signal gate. Such a variation is essential for a properly operated surface channel CCD structure.

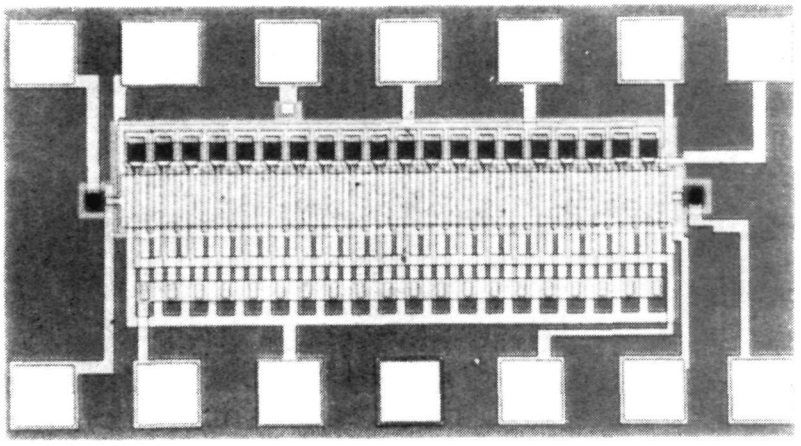


Figure 10. New 20-Element CCIRID: 8585 Design

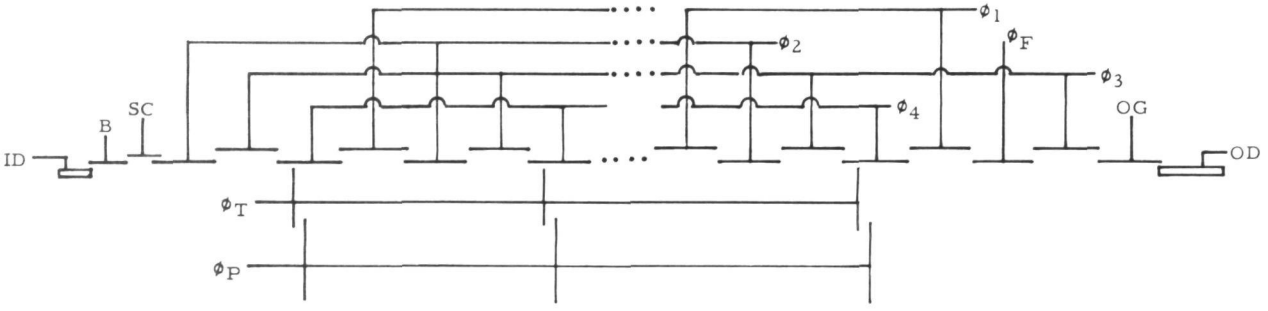


Figure 11. Schematic Diagram of 4ϕ Overlapping Gate 20-Element Imager: 8585 Design

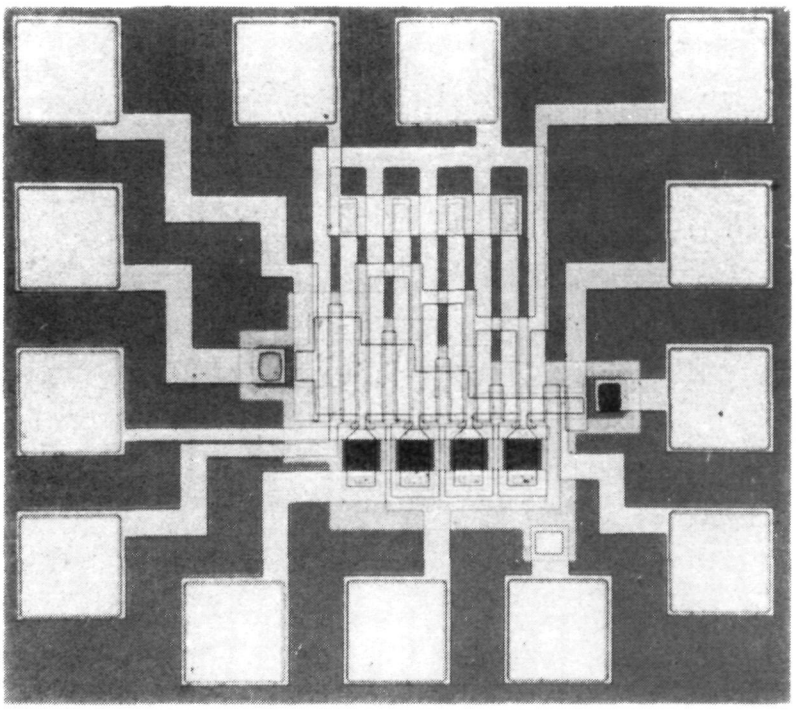
The 20 detectors are Metal-Insulator-Semiconductor (MIS) capacitors with thin ($\simeq$0.0075 μm) titanium serving as the transparent metal gate. These detectors are later contacted through a surface metal photogate (ϕ_P) bus bar

by means of a contact window in the buried metal insulator. The detector element size is 1806 μm^2 (2.8 $mils^2$) but only 1652 μm^2 (2.6 $mils^2$) is exposed to the incident photon flux. All remaining area is masked by the overlap of the photogate (ϕ_P) and transfer gate (ϕ_T) bus lines. For the detector separation, a distance of 15 μm (0.6 mil) allows room for the ϕ_2 clock line to interleave between the elements and yet still provides a reasonable detector size.

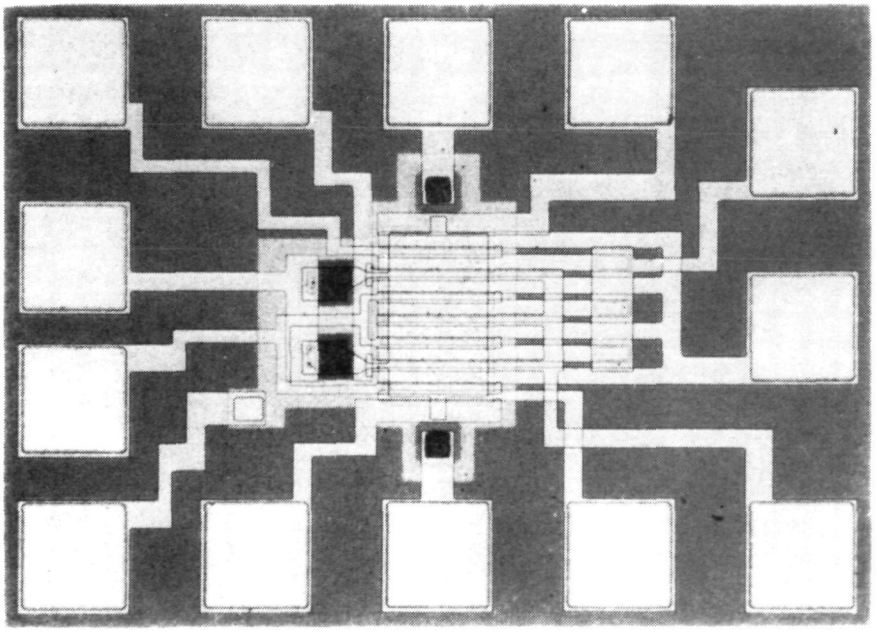
For the device output, a floating diode (OD) isolated from the CCD channel by a surface metal control gate (OG) is used. In the ideal case, the diode would be part of an "on-chip" amplification circuit such as the gated charge integrator. Since such a circuit has not been demonstrated thus far on InSb, the desire for maximum flexibility in signal detection dictated the isolated diode. In this fashion, the OD contact can be bonded directly to the on-chip GCI circuit or to an external silicon circuit if required.

Figure 12 shows both the 4-element TDI array and the 2-element, 10-μm gate length CCIRID imager. Both these structures are 4ϕ overlapping gate structures with optical and electrical input into the CCD registers also being described by Figure 11. The import of the 2-element imager is that its shorter gate lengths represent the next generation goal for CCIRID design. A demonstration of its operability and an investigation of its characteristics will thus provide information on these future designs. The TDI array is primarily intended to demonstrate this function on an InSb substrate. It is not an optimized design for any specific application, but rather includes the general TDI features in such a way as to maximize process yields.

A 2ϕ overlapping gate CCIRID is shown in Figure 13. This structure is basically the same as that of the 4ϕ design but with the $\{\phi_1, \phi_2\}$ gates of the 4ϕ structure becoming ϕ_1 in the 2ϕ device. Similarly, the set $\{\phi_3, \phi_4\}$ becomes ϕ_2 of the 2ϕ mode. Figure 14 illustrates in schematic form the basic circuit for this 4-element imager. The input structure for "fat zero" input is again of the fill and spill type. The storage gate in this case is a buried gate of the ϕ_1 clock line. Photocharge from the detectors (ϕ_P) is



(a) TDI Array



(b) 10-μm Gate Length Imager

Figure 12. Four-Element TDI Array and Two-Element (10-μm Gate Length) Imager: 8585 Chip Design

injected into the CCD readout register via the buried gate of the ϕ_2 line. It may be observed that an empty bit is inserted between detectors to evaluate "cross-talk" effects between detectors. An isolated ϕ_1 line is used for the floating clock line in this design so that, for a floating diffusion output, the ϕ_F line will be connected directly to the ϕ_1 supply.

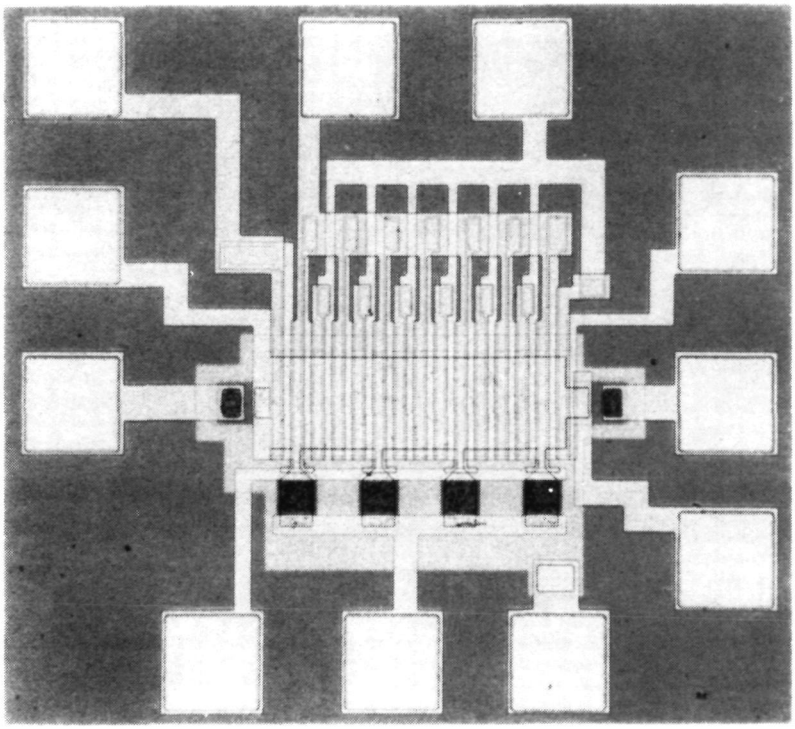


Figure 13. Four-Element 2ϕ Linear Imager: 8585 Chip Design

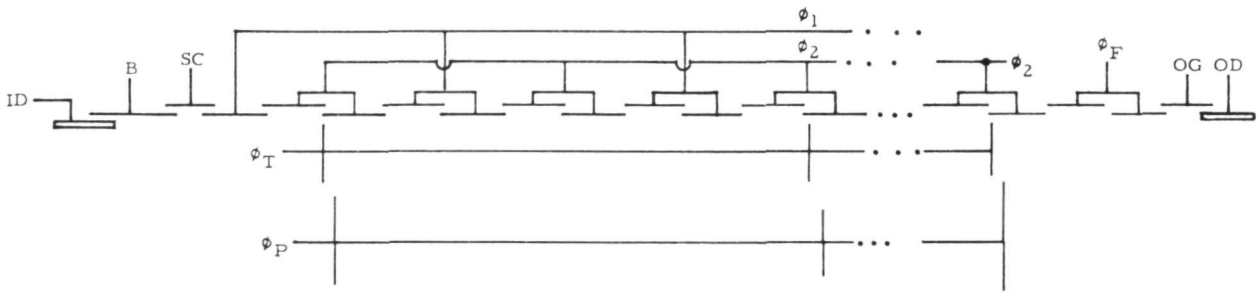


Figure 14. Schematic Circuit for 2ϕ, Four-Element CCIRID: 8585 Design

INPUT/OUTPUT CIRCUIT CONSIDERATIONS

The operation of a CCIRID can be divided roughly into three distinct functions: 1) the electrical injection of charge into the register for test and "fat zero" purposes; 2) the storage of a charge packet (fat zero charge plus photon generated charge) in individual storage wells along the CCD register; and 3) the detection of the charge packet at the CCD output. Since several new features have been added in the 8585 design which influence these functions, it is necessary to consider them in some detail.

The use of the "fill and spill" input structure[5, 6] on the 8585 has already been mentioned. In this technique, the basic components are an input diode (ID), input signal (B) gate, and a signal storage gate (ST). In addition, a surface control (SC) gate is required in overlapping gate structures as will be clear from the following discussion. Figure 15 shows the basic schematic format of this input scheme, together with the requisite phasing of the input clocks and the surface potential profiles at different instants of time during the input cycle. From the figure, it is clear that the injected charge (Q_{inj}) is proportional to the difference in surface potentials between gates B and ST.

But the surface potential, as a function of applied gate voltage, can be written for a large (fringe effects can be ignored) MIS capacitor as

$$\psi_s = V_o + V - (V_o^2 + 2V\ V_o)^{\frac{1}{2}} \qquad (3)$$

where

$$V_o = -\frac{q\gamma\epsilon_s N_s}{C_{ox}^2} \quad \text{and} \quad V = V_G - V_{FB} - \frac{q_o}{C_{ox}}$$

---

5. M. Tompsett, IEEE Trans. Electron Devices, V. ED-22, p 305, June 1975.

6. S. P. Emmons and D. D. Buss, J. of Applied Physics, V. 45, p 5303, December 1974.

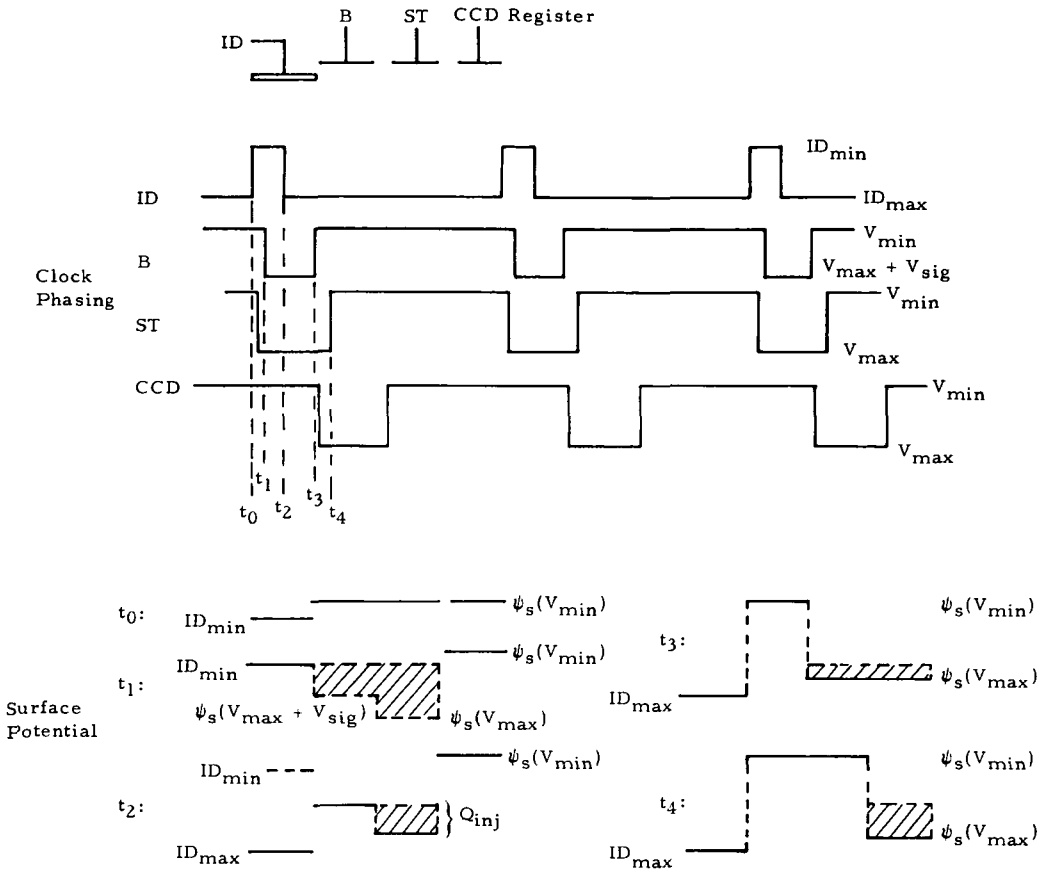


Figure 15. Fill and Spill Input Circuit, Schematic Diagram, Clock Phasing, and Surface Potential

In these expressions, C_{ox} is the oxide capacitance/unit area of the storage gate, N_s is the substrate doping level, ϵ_s is the substrate permittivity, and γ is a constant which is +1 for n-type substrates and -1 for p-type. The quantity V_G is the applied gate voltage, V_{FB} the flat-band voltage which contains the contribution of oxide fixed (Q_{FC}) charge, and q_o is inversion charge stored at the interface. In principle, this quantity also contains interface state charge, but this point is not important for the present argument.

Using Figure 15, it is apparent that when $q_o = Q_{inj}$, then

$$\psi_s(B) = \psi_s(ST) \tag{4}$$

where B and ST refer to the surface potential under discussion. From equation (3) and the physical observation that

$$q_o(B) = 0 \qquad q_o(ST) = Q_{inj}$$

then

$$V_{oB} - V_{GB} - V_{FB}(B) - \left\{V_{oB}^2 + 2V_{oB}\left[V_{GB} - V_{FB}(B)\right]\right\}^{\frac{1}{2}} = V_{oST} + V_{GST}$$

$$- V_{FB}(ST) - \frac{Q_{inj}}{C_{oxST}} - \left\{V_{oST}^2 + 2V_{oST}\left[V_{GST} - V_{FB}(ST) - \frac{Q_{inj}}{C_{oxST}}\right]\right\}^{\frac{1}{2}} \quad (5)$$

Now, V_{oB} and V_{oST} differ only in the oxide capacitance term being for gate B in the first case and gate ST in the second. Since

$$V_{GB} = V_{max} - V_{sig} \qquad V_{GST} = V_{max} \quad (6)$$

it follows from equation (5) that a formal identity arises if $C_{ox} = C_{oxB} = C_{oxST}$ (same oxide thickness under B and ST gates) for then one must have

$$-V_{sig} = -\frac{Q_{inj}}{C_{ox}}$$

or

$$Q_{inj} = C_{ox}\, V_{sig} \quad (7)$$

Hence, the injected charge in this input scheme varies linearly with the impressed signal voltage.

This result depends strongly on several assumptions. First, it is assumed that the coupling between the B and ST storage wells is perfect, i.e., there is no charge loss or storage in the region between these gates. In actual fact, however, it is known that gaps of 0.5 μm or less can introduce irregularities (glitches) in the surface potential profile which links B and ST. These glitches can destroy the relation given in equation (7) so, in the absence of very narrow gaps (≤0.1 μm), it is imperative that some means of control be established over the potential profile in the gap region. One approach is to use a gate, on a different level than B and ST, and with which the gap region is biased such that optimum conditions exist in this region. If the gap is made as small as practicable, this approach will yield a result closely given by equation (7). An alternative concept uses a floating diffusion to

accomplish the connection between B and ST. This concept is as valid as that of an overgate, and the choice is dependent primarily on the technology available. In the 8585 design, the overgate concept has been used.

It is also clear that equation (7) is definitely invalid if the respective oxide capacitance terms, C_{oxB} and C_{oxST}, are not the same. Under the latter condition, the charge injected is related to V_{sig} in a complicated, nonlinear fashion. It follows that the fill-and-spill approach must have both the signal and storage gates on the same oxide thickness in order for the simple linear relationship to hold. Finally, it is clear that the storage gate ST could be eliminated and the charge injected directly into the CCD register gate. This approach has been adopted for the 8585 design.

The storage capability of a 4ϕ CCD register is limited only by the breakdown voltages of the device insulators as the gates can be selectively clocked from their threshold value to the breakdown value. For a 2ϕ stepped oxide device, however, the storage capacity is determined by the difference of the oxide thicknesses. In fact, if the upper and lower gate insulator thicknesses are designated by t_U and t_L respectively, then the charge capacity per unit area of a 2ϕ stepped oxide well is given by

$$Q_{max} = \delta\left[-\frac{q\gamma\epsilon_s N_s}{C_{oxL}}(\delta + 2) + Q_{FC}\right] + \sqrt{L} - \sqrt{U} \qquad (8)$$

where

$$\delta = \frac{t_U - t_L}{t_L}$$

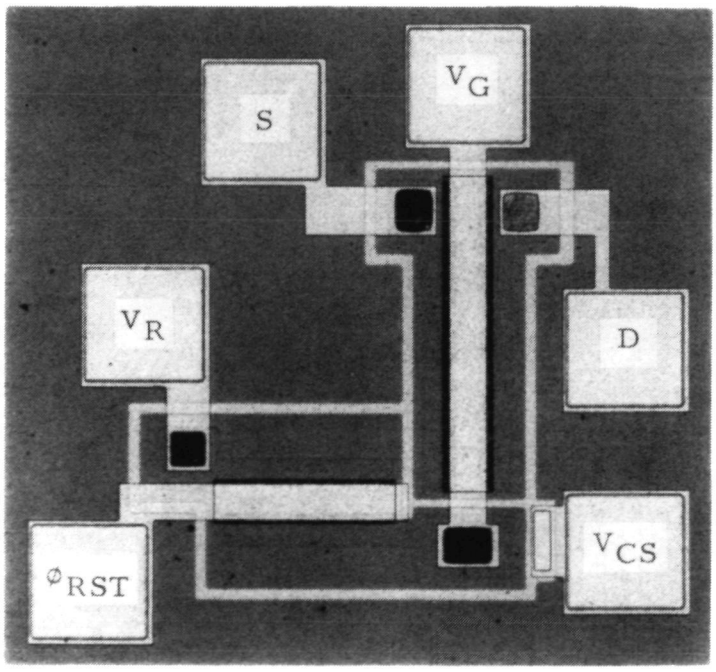
and

$$\sqrt{L} - \sqrt{U} = [V_{oL}^2 + 2V_{oL}(V_G - V_{FBL})]^{\frac{1}{2}} - [V_{oU}^2 - 2V_{oU}(V_G - V_{FBU})]^{\frac{1}{2}}$$

The parameters V_{oL} and V_{FBL} are defined by equation (3) but with the proper oxide capacitance/unit area inserted. Equation (8) assumes the same fixed oxide charge Q_{FC} under both the upper and lower gates with the same gate bias V_G applied to each. Beyond these constraints, the result is valid to within the limits of the depletion approximation and the neglect of fringe field effects at the gate edges. It is clear that, in operation, the fill-and-spill

input must be properly adjusted to account for the smaller (in general) storage capacity of a 2ϕ device in comparison with a 4ϕ structure. The validity of these arguments will be examined on the 8585 chip via the 4-element 2ϕ device.

The final detection of charge at the device output can be accomplished on the 8585 devices either by using a floating diode or a floating "clock" line. In both cases, the detection consists of observing the voltage change on a capacitance (the diode or floating clock) when charge from the CCD register is deposited onto the capacitance. The basic equations are given by (1) and (2) and need not be repeated here. It is sufficient to note that the gated charge integrator of Figure 16 allows "on-chip" detection of this voltage charge. At the same time, the ready accessibility of the output diodes allows use of an external amplifier if the monolithic circuit is not operative.



V_G	Output Diode
S	Source
D	Drain
V_R	Preset Reference
ϕ_{RST}	Reset Gate
V_{CS}	Channel Stop
SUB	InSb Substrate

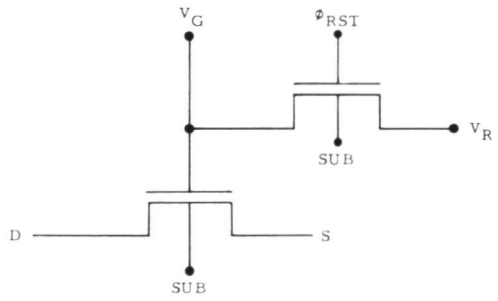


Figure 16. Monolithic Source-Follower Reset Circuit (Gated Charge Integrator) Included on 8585 Chip

Section 4

SYSTEM STUDY: MONOLITHIC InSb CCD ARRAY FOR AN EARTH RESOURCES SENSOR

Several applications exist in the fields of remote earth sensing and planetary exploration for which the use of InSb CCD monolithic focal plane arrays with TDI would increase system performance. A partial list of potential applications includes forest fire surveillance and mapping, atmosphere temperature sounding in the 4.3-μm CO_2 band, pollution monitoring, mineral exploration and other geological uses, and distinguishing between clouds and water surfaces, all of which present mid-IR (1 to 5 μm) signatures. To estimate a representative level of performance improvement that should be realized with these arrays, a future generation Landsat Sensor has been considered using a monolithic InSb TDI CCD focal plane, and its performance has been calculated.

Such a future Landsat Sensor configuration is shown in Figure 17. This sensor system utilizes (intrinsic) silicon detectors on a warm focal plane for reflected light bands and one or more InSb TDI CCD arrays on a cold (95°K) focal plane for mid-IR bands. Other arrays may also be included on the cold focal plane for long-wavelength IR bands.

The Landsat spacecraft is assumed to be positioned in a sun-synchronous orbit at 705 km altitude. The IFOV of the system is 42 μrad giving a ground resolution of 30 meters, an improvement of a factor of 2.5 over the present multispectral scanner systems (MSS) now in orbit. A scan mirror (Figure 17) scans the linear arrays in the perpendicular-to-track direction to produce a 185-km swath width. This scan motion allows on-focal-plane TDI to be readily implemented without changing the basic sensor configuration.

The focal plane organization for the InSb TDI CCD array is shown in Figure 18. The number of detectors in TDI is 16; thus, the array is 16×16 or 256 elements total. The selection of a 16-element TDI subarray is not

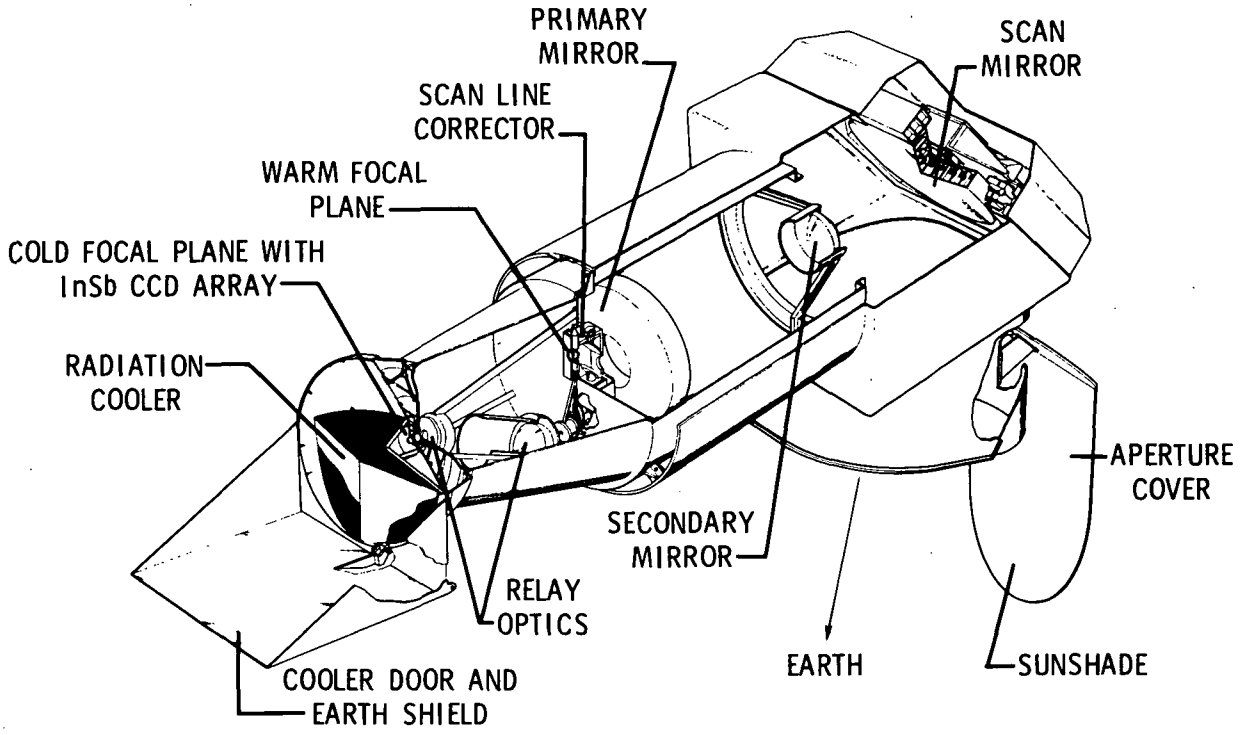


Figure 17. Future Generation Landsat Sensor with InSb CCD Focal Plane

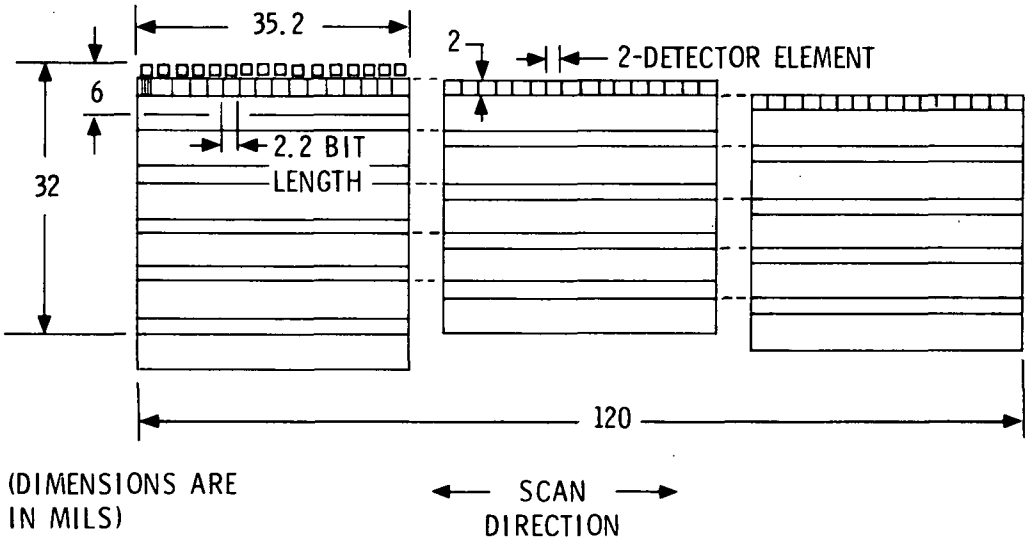


Figure 18. Focal Plane Organization for 16×16 InSb TDI CCD Array

necessarily optimum; for this choice, the subarray detectivity in the ideal case is $\sqrt{16}$ = 4 times the individual detector D*. Since the performance improvement is proportional to the square root of subarray length, relatively small gains are achieved by using numbers of detectors greater than about 30.

The 16 subarrays are aligned with the perpendicular-to-track direction and staggered as shown in Figure 18 to provide contiguous coverage in the along-track direction.

The InSb CCD array parameters and the system parameters assumed for the future Landsat Sensor are given in Table 1. The two spectral bands considered are a 1.55- to 1.75-μm band and a 3.6- to 4.1-μm (atmospheric window) band. Detectors are 0.05-mm (0.002-inch) square for the 42-μrad IFOV and telescope parameters assumed. The InSb CCD parameters are listed in the lower half of Table 2. These are based on typical design values and measured material parameters and represent presently achieved values or those predicted for the near future. Because of the relatively low backgrounds and scene radiances in these spectral bands and system dwell time,

Table 1. InSb CCD Array Parameters and Representative System Parameters for Future Landsat Sensor

SYSTEM	InSb SPECTRAL BANDS		1.55 TO 1.75 μm 3.6 TO 4.1 μm
	ORBIT ALTITUDE		705 km
	ORBITAL PERIOD		98.5 minutes
	IFOV		42 μrad
	CROSSTRACK SWATH		0.26 rad
	f/NO.		f/3
	FOCAL LENGTH		1.2 meters
	OPTICAL EFFICIENCY		0.5
	DETECTOR AREA	A_D	2.58×10^{-5} cm^2
	SAMPLE RATE		1/RFOV
	FOCAL PLANE TEMPERATURE	T	95°K
	NO. OF DETECTORS PARALLEL-TO-TRACK		16
DETECTOR/ CCD	QUANTUM EFFICIENCY	η	0.75
	CCD BITS/DETECTOR		1
	BIT LENGTH		56 μm
	BIT AREA	A_B	1.42×10^{-5} cm^2
	THIN OXIDE CAPACITANCE		4×10^{-8} f/cm^2
	CLOCK VOLTAGE		5 volts
	DARK CURRENT (95°K)	J_D	10 μa/cm^2
	INTERFACE STATE DENSITY	N_{SS}	10^{11}/cm^2-eV
	INPUT/OUTPUT CAPACITANCE	(C_{IN}, C_O)	0.5 pF
	OUTPUT DEVICE NOISE AT 1 Hz	V_1	12.5 μV/ $\sqrt{Hz}$

the CCD bit area required is not large, nor is it necessary to taper the CCD register in this case as needed in some TDI applications. This results in the compact array configuration shown in Figure 18.

Table 2. Detectivity Calculations for Conventional and InSb TDI CCD Arrays

		SPECTRAL BAND (μm)			
		1.55 TO 1.75		3.6 TO 4.1	
RESPONSIVITY (a/w)	R	1.0		2.3	
BACKGROUND PHOTON FLUX (photons/sec cm^2)	Q_B	NEGLIGIBLE		7.4×10^{13}	
NUMBER OF DETECTORS PERPENDICULAR-TO-TRACK	N	1*	16**	1*	16**
SCAN EFFICIENCY		0.8	0.4	0.8	0.4
IFOV DWELL TIME (μsec)		9.0	4.5	9.0	4.5
BANDWIDTH (kHz)	Δf	55	110	55	110
CLOCK FREQUENCY (kHz)	f_C	---	220	---	220
DETECTOR TYPE		PV InSb	InSb CCD WITH PHOTOGATES	PV InSb	InSb CCD WITH PHOTOGATES
PREAMPLIFIER		CURRENT-MODE	NONE	CURRENT-MODE	NONE
DETECTOR DYNAMIC IMPEDANCE (Ω)		6×10^8	---	6×10^8	---
SHORT CIRCUIT CURRENT (a)		NEGLIGIBLE	---	2.3×10^{-10}	---
FEEDBACK RESISTANCE (Ω)		2×10^7	---	2×10^7	---
EXCESS NOISE CURRENT (a/$\sqrt{\text{Hz}}$)		3×10^{-15}	---	3×10^{-15}	---
TOTAL NOISE (a/$\sqrt{\text{Hz}}$)		1.7×10^{-14}	---	1.9×10^{-14}	---
NOISE ELECTRONS:					
PHOTON	N_P	---	NEGLIGIBLE	---	321
RESET	N_{RST}	---	130	---	130
DARK	N_D	---	385	---	385
FAT ZERO	N_{FZ}	---	130	---	130
INTERFACE STATE	N_{FIS}	---	358	---	358
OUTPUT DEVICE	N_{OUT}	---	140	---	140
TOTAL	N_T	---	574	---	658
D^*_λ (cm Hz$^{\frac{1}{2}}$/watt)		3.0×10^{11}	1.3×10^{12}	6.2×10^{11}	2.7×10^{12}
D^*_{BLIP} (η = 0.75)		---	---	1.4×10^{12}	5.5×10^{12}

$$N_P^2 = N\eta Q_B A_D T_C \qquad N_{FIS}^2 = 0.69 \frac{kT}{q} A_{CCD} N_{SS}$$

$$N_{RST}^2 = 2kTC_O/3q^2 \qquad N_{OUT}^2 = (V_1 C_O/q)^2 \ell n(1/T_C)$$

$$N_D^2 = \left[\frac{NJ_D T_C}{q}(A_D + \tfrac{1}{2}A_B)\right] \qquad D^*_\lambda = \left(\frac{A_D T_C}{2}\right)^{\frac{1}{2}} \frac{N\eta\lambda}{hcN_T}$$

$$N_{FZ}^2 = 2kTC_{IN}/3q^2$$

*CONVENTIONAL SYSTEM **TDI CCD

Using these parameters, the results of D* calculations for the two spectral bands are given in Table 2. In each spectral band, detectivity is calculated for: 1) a conventional system configuration with a 16-element (i.e., one detector/IFOV in the perpendicular-to-track direction); and 2) the 16×16 InSb TDI CCD array. The conventional system utilizes PV InSb detectors and current-mode preamplifiers. Noise and D* for this array were calculated using the usual noise current formalism. For the InSb TDI CCD, detectivity was calculated based on noise variance estimates for detector, CCD, and output circuit sources as tabulated in the second and fourth columns of Table 2.

In both bands, the InSb TDI CCD is shown to offer a significant detectivity improvement. For the conventional detector array, D* is amplifier/feedback resistance noise limited in both bands. In the 3.6- to 4.1-μm band, for example, D* is about 45% of the BLIP value for the PV InSb discrete amplifier case. For 16 elements in TDI, the ideal BLIP D* is four times higher. The estimated InSb TDI CCD D* in the 3.6- to 4.1-μm band is, with all noise variances considered, about 50% of this limit. Effective performance in this band is improved by a factor of 4 through use of the monolithic InSb TDI array.

In the 1.55- to 1.75-μm band, thermal background radiation is negligible and reflected sunlight dominates scene radiance. It is instructive to examine the improvement in system SNR in this band when InSb TDI CCDs are used. The minimum radiance N_{min} in this band is approximately 80 $\mu w/cm^2$-sr. Using a clear aperture area for the telescope equal to 85% of the primary mirror area and other optical parameters in Table 1, this radiance results in a power 7.8×10^{-11} watts, or 6.5×10^{8} photons/sec, imaged on each detector. The summed signal charge at the TDI CCD output is $16\times0.75\times6.5\times10^{8}$ $\times4.5$ μsec $= 3.5\times10^{4}$ charges. Including shot noise in signal, the total noise electron count is 604 electrons, yielding SNR = 58 at the minimum radiance level. For the single detector case, using R = 1 a/w, the noise current in Table 2, and including signal shot noise, the corresponding SNR at N_{min} is 19.

These calculations illustrate the potential impact of InSb CCD arrays on future spacecraft sensor systems.

Section 5

CONCLUSIONS

The following conclusions may be drawn from the results of this contractual effort:

1. The redesign of the buried metal, buried metal insulator, and surface metal photomask layers of the 8582 has eliminated the previously reported problems of "microcracks" in the surface metal clock lines.
2. The use of reverse photolithography, even with the 8582 redesign, continues to limit device yields by leading to almost total breakage of the buried metal clock lines at the CCD channel edge as defined by the channel stop insulator.
3. A process (Buried Channel Stop) to eliminate the channel stop insulator and to alleviate this breakage has been developed, and was shown to be successful. It suffers from requiring very high quality insulators due to the thin layers utilized in the process.
4. The desired total etch technology is incompatible with the 8582 design barring almost a complete redesign of all remaining photomask layers.
5. A new CCIRID chip (8585) has been designed which corrects the errors heretofore observed in the 8582 design. The new design incorporates 1) a 20-element 4ϕ linear imager with 12.5-μm gate lengths; 2) a 4-element 4ϕ TDI array and a 4-element 2ϕ linear imager with 12.5-μm gate lengths; 3) a 2-element 4ϕ linear imager with 10.0-μm gate lengths; 4) a monolithic gated charge integrator circuit for on-chip signal processing; and 5) an assortment of test devices.
6. A system study of a future Landsat Sensor system configured around an InSb TDI array has been considered. In the band 3.6- to 4.1-μm, the calculated detectivity (D*) values are a factor of four greater than the corresponding conventional detector arrays.

Beyond these direct observations, it must be emphasized that both internal and external (in particular, the HALO Monolithic Intrinsic Detector/MUX Array Program, No. F04701-76-C-0174) funding have enabled extensive improvements in processing capability and promise near-term achievement of a total etch CCIRID technology. The result for the NASA CCIRID program is clearly advantageous as these improvements ensure a significant reduction in the development time required for space qualified infrared CCD imagers.